REMARKS

In response to the Office Action mailed July 3, 2007, Applicant respectfully requests reconsideration. Claims 1-10 were previously pending in this application. By this amendment, Applicant is canceling claim 3 without prejudice or disclaimer. Claims 1 and 7 have been amended herein. New claims 11-28 have been added. As a result, claims 1, 2 and 4-28 are pending for examination with claims 1, 7, 11 and 19 being independent. No new matter has been added.

Allowable Subject Matter

As a preliminary matter, Applicant notes with appreciation the indication of allowable subject matter in claims 9 and 10.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 1-6 under 35 U.S.C. 112, second paragraph, as being indefinite because the element "the second electrode" in claim 1, line 3, lacked antecedent basis. Claim 1 has been amended to recite, *inter alia,* "A capacitor having first and second electrodes." As a result, proper antecedent basis now exists for the second electrode(s) recited in claims 1 and 4. Accordingly, withdrawal of these rejections is respectfully requested.

Rejections Under 35 U.S.C. §102

A. Independent Claim 1

The Office Action rejected claims 1-3 under 35 U.S.C. 102(b) as being purportedly anticipated by Kishi et al., U.S. Patent No. 5,302,542. Applicant respectfully requests reconsideration.

Kishi relates to a DRAM cell that includes a transfer transistor and a trench capacitor (Abstract). As illustrated in FIG. 6 of Kishi, the transfer transistor is positioned to the side of the trench capacitor. The P-type doped region 21 of the transfer transistor is electrically connected to the P-type electrode 18 of the trench capacitor by epitaxial layer 20 (Col. 4, lines 15-19). Electrode 18 is formed in the substrate 11 and is separated from the substrate by a silicon oxide

dielectric film 17 (Col. 3, lines 35-64). As seen from the foregoing, Kishi's trench capacitor establishes a capacitance between P-type electrode 18 and the substrate 11.

By contrast, claim 1 as amended recites, *inter alia*, a capacitor dielectric disposed under said drain or source region. Kishi does not teach or suggest a capacitor dielectric disposed under a drain or source region. Rather, as illustrated in FIG. 6, Kishi's dielectric film 17 is located to the right of both the drain and source regions, not disposed under either a drain or a source region. Therefore, claim 1 patentably distinguishes over Kishi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-6 depend from claim 1 and are therefore patentable for at least the same reasons.

B. Independent Claim 7

The Office Action rejected claims 7 and 8 under 35 U.S.C. 102(b) as being purportedly anticipated by Lu, U.S. Patent No. 5,843,820. Applicant respectfully requests reconsideration.

Lu describes a method of forming a DRAM cell having an access transistor and a trench capacitor (Abstract). As illustrated in FIGS. 6-7 of Lu, a high-k dielectric layer 40 is formed in a trench of P+ substrate 40. A polysilicon region 50 is then formed in the trench on the high-k dielectric layer 40 (Col. 7, line 53 – Col. 8, line 8). A second high-k dielectric layer 52 is formed on top of polysilicon region 50, and region 52 is etched so that region 52 only remains near the edges of the trench capacitor (Col. 8, lines 17-30). As illustrated in FIG. 9 of Lu, an epitaxial layer 54 is grown above the trench capacitor (Col. 8, lines 8-52). FIGS. 10 and 11 of Lu illustrate that a node contact hole 9 is etched into epitaxial layer 54. A liner oxide 64 is formed on the sidewalls of the node contact hole 9, and then node contact hole 9 is filled with a polysilicon layer 66 (Col. 9, lines 5-33). Source/drain contact areas 17 of the access transistor FET are formed adjacent to the trench capacitor (Col. 10, lines 10–25). As illustrated in FIG. 12 of Lu, a source/drain contact area 17 is formed above the trench capacitor at the surface of epitaxial layer 54.

The Office Action relies on source/drain region 17 and polysilicon regions 50/66 of Lu as purportedly forming different electrodes of a capacitor. However, as should be appreciated from Lu, particularly at Col. 7, lines 33-52, Lu's trench capacitor establishes a capacitance between the polysilicon region 50 and the underlying substrate, not the source/drain region 17. Lu states

that the capacitance is dependent on the shape of the trench formed in the substrate (Col. 7, lines 33-52). However, Lu makes no mention of a capacitor being formed between a source/drain region 17 and polysilicon region 50/66. In fact, Lu states that a source or drain region 17 of the access transistor is electrically connected to polysilicon layer 66 (and thus region 50) via node strap 68, which is a conducting layer (Col. 10, lines 26-27, FIG. 12).

By contrast, claim 7 as amended recites, *inter alia*, forming said heavily-doped active region across the entire thickness of said semiconductor layer, above a portion of the coated conductive region, the heavily-doped active region being insulated from the conductive region. Lu does not teach or suggest this limitation of claim 7 because the source/drain region 17 of Lu is electrically connected to the polysilicon capacitor electrode 50. In view of the foregoing, claim 7 patentably distinguishes over Lu. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 8-10 depend from claim 7 and are therefore patentable for at least the same reasons.

New Claims

New claim 11 recites, *inter alia*, at least one capacitor comprising a first electrode comprising a drain or source of a MOS transistor; a first capacitor dielectric region having at least a portion that contacts the first electrode and is buried beneath the first electrode; and a second electrode buried beneath the first electrode, the second electrode being insulated from the first electrode. The art of record does not teach or suggest these elements. Claim 11 patentably distinguishes over Kishi and Lu because the regions of these devices relied upon in the Office Action (for the rejections of independent claims 1 and 7) are not insulated from one another, but rather are electrically connected.

Claims 12-18 depend from claim 11 and are therefore patentable for at least the same reasons.

New claim 19 recites, *inter alia*, forming a heavily-doped active region in the semiconductor region above the at least a first portion of the insulating region such that the heavily-doped active region contacts the at least a first portion of the insulating region, wherein the second electrode comprises the heavily-doped region, wherein the first and second electrodes are insulated from one another. The art of record does not teach or suggest these limitations.

Claim 19 patentably distinguishes over Kishi and Lu because the regions of these devices relied upon in the Office Action are not insulated from one another, but rather are electrically connected.

Claims 20-28 depend from claim 19 and are therefore patentable for at least the same reasons.

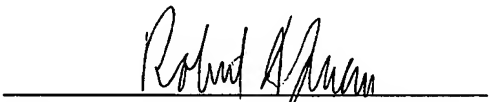
CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: January 3, 2008

Respectfully submitted,

By: 

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